

Jayadevan (Jay) Radhakrishnan

121 Holiday Road, Rochester, NY 14623

Email: jxr6107@rit.edu, Cell: (585)944-7326

OBJECTIVE:	To establish a Full-Time career utilizing current design and development applications in Electrical Engineering.
EDUCATION:	Rochester Institute of Technology, Rochester, NY BS/MS in Electrical Engineering, May 2009 GPA: 3.5/4.0
AWARDS:	Dean's List Award, RIT Merit Scholarship Recipient, Lean Six Sigma Yellow Belt
COMPUTER SKILLS:	<i>Operating Systems:</i> Windows (NT, 2000, XP, Vista), UNIX, MAC OS, Linux <i>Languages:</i> C, C++, Assembly, STL, Visual Basic, VHDL, Python <i>Networking / Communication Protocols:</i> IP Version 4, MODBUS, OPC <i>Applications / Tools:</i> Matlab, Labview, Simulink, ModelSim, Quartus 5.0, Cadstar, Cadence, Tricon 1131, Allen-Bradley RS Logix 500, GE Speedtronic Mark VI Toolbox, GE Fanuc Cimplicity, Emerson DeltaV, MS Office, Altera Max II Plus, Visio, Orcad, PSpice, Adobe Acrobat, Adobe Photoshop, PCB123 Schematic, PCB123 Layout, Oracle, VMWare
COURSEWORK:	Digital Signal Processing, State Space Control, Digital Image Processing, Adaptive Signal Processing, Robust Control, Pattern Recognition, Fuzzy Logic and Applications, Mechatronics, Design of Digital Systems, Matrix Methods in EE, Random Signals and Noises, Mixed Signal IC Design, Linear Systems I & II, Electromagnetic Fields I & II, Communication Systems
PROJECTS:	
<i>Control Systems Design:</i>	Modeling the Permanent Magnet DC Motor, Performance Analysis of Open-Loop and Closed-Loop Systems, Transient Response and Design Parameters, Effect of Additional Pole and/or Zero, Effect of Adding a Pole and/or Zero within the Loop, Velocity of the DC Motor Using Compensators
<i>Robust Control:</i>	Robust Control Design of a Magnetic Levitation System
<i>Digital Image Processing:</i>	Circular Symmetric Watermark Embedding, Image Enhancement Filters, Image Restoration Filter Design, Histogram Processing, 2D and 3D Object Manipulation, 2D Filtering in DFT Domain
<i>Pattern Recognition:</i>	Classification using Gaussian distribution, Multiple Class Classification, K Means & Fuzzy K-Means Clustering, and Eigenfaces for Recognition, KL Expansion for an Invariant Feature Space, Texture Analysis and Classification using Tree-Structured Wavelet Transform, Image Segmentation using DWF
<i>Senior Design Project:</i>	Wireless Assistive Control System – Control System Design, Prototype/New Product Design
<i>Digital Electronics:</i>	Design, Simulation /Testing of NMOS Inverters, CMOS Inverter and CMOS Combinational Logic, CMOS Sequential Logic, Propagation Delay through CMOS Logic, Dynamic CMOS Logic, MOS-based Memory Ripple Counters (Altera Max), Versatility of Hardware Devices, NAND Logic Design, Multiplexers, Basic Latches and Flip Flops
<i>Digital Systems:</i>	
<i>Microcomputers:</i>	Keypad Scanning Using Input/Output Ports, Peripheral Control, Controlling the Seven- Segment Display
<i>Computer Architecture:</i>	ALU Design, Registers, Counters and RAM, Processor Datapath, Control Unit, Complete Processor Simulation and Emulation
<i>Electronics I (BJTs):</i>	Diode characteristics and Circuits, BJT characteristics, Biasing and Amplifiers, Power Supply Design, Transistor Modeling of BJTs, BJT Common Emitter Amplifier Design
<i>Electronics II (MOSFETs):</i>	MOSFET Characterization, MOSFET Current source MOSFET Differential Pair with Resistive Load, MOSFET Differential Pair with Active Load, Feedback Amplifier & Stability
WORK EXPERIENCE:	Xerox Corporation, XIG/XRCW/DWSL/CICS, Webster, NY (07/2008-11/2008) Electrical Engineering Coop Assisted X SIS with Architecture Designs, System Integration, Embedded Programming & Application Development for the Perle ACQ project MKS Instruments, Software and Controls Dept., Rochester, NY (11/2006-05/2007) Coop-Intern Assisted software engineering with the following jobs: Generate/Revise/Update Schematics, Bills of Material, Test Fixtures, Reliability Stress Sheets, Printed Circuit Layout, Software Design/Development, Digital Circuit Design, Board Designs, Embedded Programming Yokogawa Middle East, Engineering Dept., Bahrain (10/2006-11/2006) Engineering Assistant Participated in the Factory Acceptance Test (FAT) of control system upgrade for Saudi Aramco's Uthmaniyah GOSP-7 Project Summit Technologies, Instrumentation and Process Control Dept., Al-Khobar (03/2005-08/2005) Engineering Assistant Worked on configuring the following systems: Tricon Version 9.0 TMR, Allen-Bradley SLC500, GE Speedtronic Mark VI gas turbine controls, GE Fanuc Cimplicity HMI, Yokogawa CENTUM CS3000 (Vnet/IP), Foundation Fieldbus (DeltaV and CS3000 implementations)
ACTIVITIES:	Institute of Electrical and Electronics Engineers (IEEE), Instrumentation Systems and Automation (ISA), RIT Fencing Club, RIT Orientation Program, Golf, DSS Labs (Lab Assistant), BLL (Research Assistant)